MFC/MFA/MFK/MFX800A
THYRISTOR/DIODE MODULE

Features

Isolated mounting base 2500V

Increased power cycling capability

Space and weight savings

$I_{T(AV)}$	800A
V_{DRM}/V_{RRM}	400-2600 V
I_{TSM}	16KA
I^2T	1280KA^{2}S

Application

AC/DC Motor drives

Various rectifiers

DC supply for PWM inverter

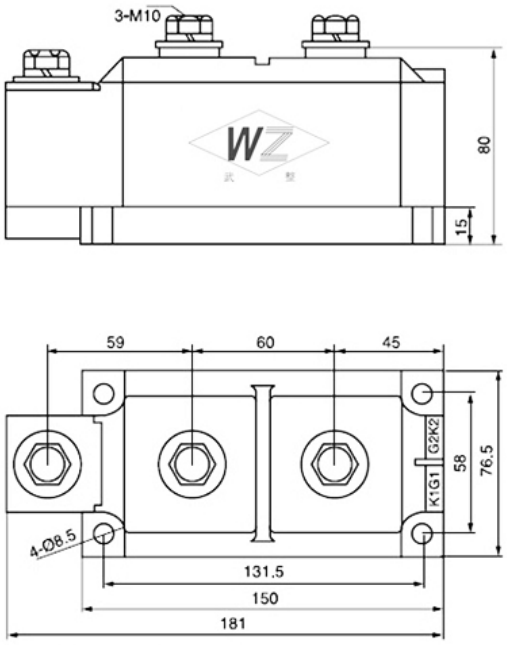
Symb.		parameter	Test Conditions	$T_{J(℃)}$	Value	Unit
Current Ratings	$I_{T(AV)}$	average on-state current	180 °half sine wave 50Hz Single side cooled Tc=85 ℃	125	800	A
	$I_{T(RMS)}$	RMS on-state current		125	1256	A
	I_{TSM}	Surge on-state current	10ms half sine wave V_R=0.6VRRM	125	16.0	KA
	I^2t	I2T for fusing coordination		125	1280	KA^{2}S
Characteristics	V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V_{DRM}&V_{RRM} tp=10ms V_{DSM}&V_{RSM}= V_{DRM}&V_{RRM}+100V	125	400-2600	V
	I_{DRM} I_{RRM}	Repetitive peak current	V_{DM}= V_{DRM} V_{RM}= V_{RRM}	125	Max.40	mA
	V_{TO}	Threshold voltage		125	Max.0.80	V
	V_{TM}	Peak on-state voltage	I_{TM}=2400A	25	Max.1.95	V
	r_T	On-state slop resistance		125	Max.0.42	mΩ
	I_H	Holding current	V_A=12V, I_A=1A	25	20-200	ma
Dynamic Parameters	dv/dt	Critical rate of rise of off-state voltage	V_{DM}=67%VDRM	125	Max.800	V/μs
	di/dt	Critical rate of rise of on-state current	I_{TM}=1200A, Gate pulse tr ≤0.5μs I_{GM}=1.5A	125	Max.100	A/μs
Gate Parameters	I_{GT}	Gate trigger current	V_A=12V, I_A=1A	25	30-200	mA
	V_{GT}	Gate trigger voltage		25	1.0-3.0	V
	V_{GD}	Non-trigger gate voltage	V_{DM}=67%V_{DRM}	125	Min.0.2	V

Thermal &Mechanical Data

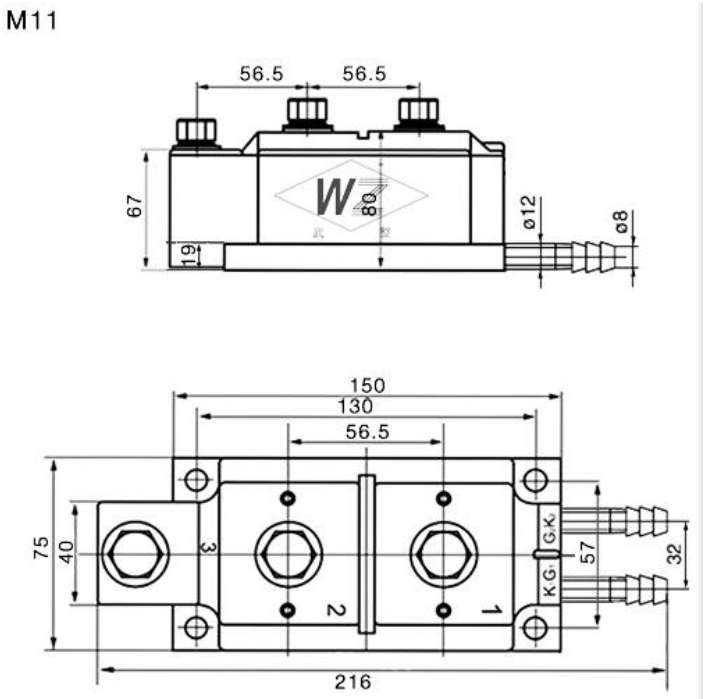
Symb.	parameter	Test Conditions	Value	Unit
$R_{th(j-c)}$	Thermal resistance Junction to case	single side cooled	Max.0.054	℃/W
$R_{th(c-h)}$	Thermal resistance case to heat sink	single side cooled	/	℃/W
V_{iso}	isolated voltage		Min.2500	V
F_m	Thermal connection torque(M5)		Typ.12	N m
	Mounting force (M6)		Typ.6	N m
T_{stg}	Stored temperature		-40-+125	℃
W_t	Weight		2600	g

Outline:

M7



M11



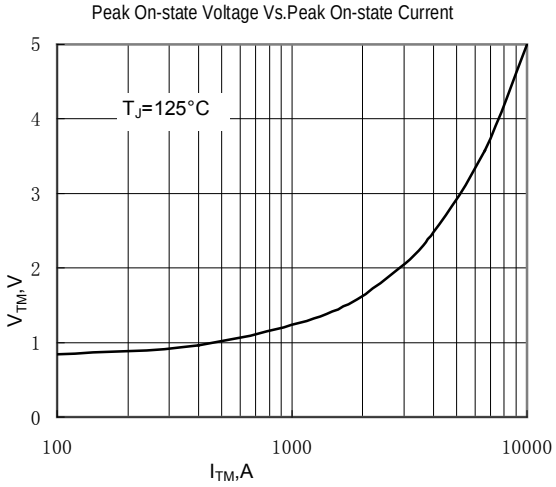


Fig.1

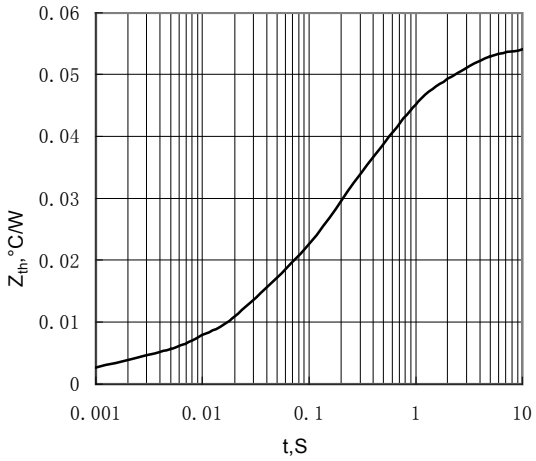


Fig.2

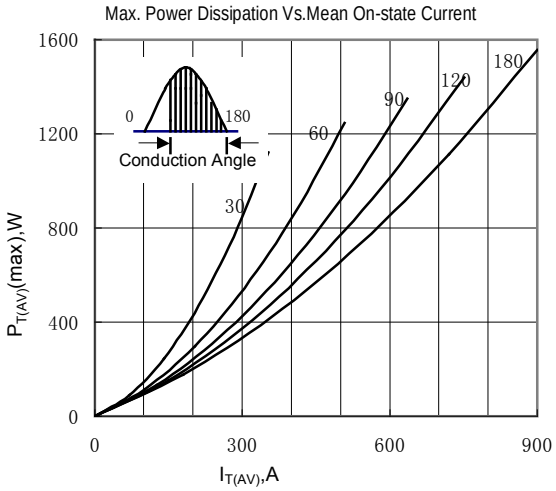


Fig.3

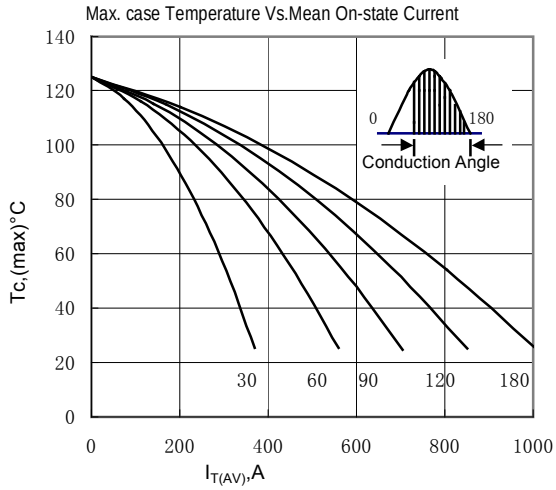


Fig.4

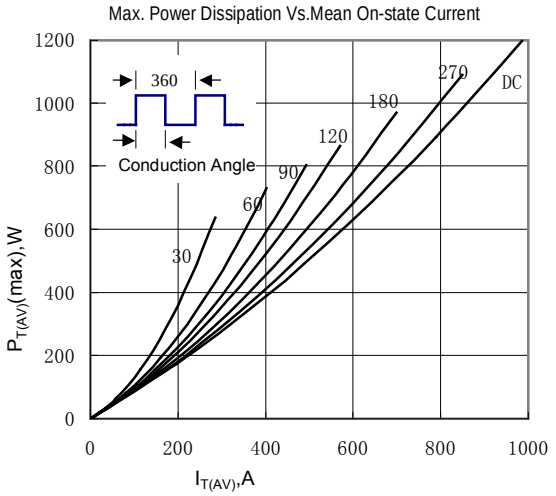


Fig.5

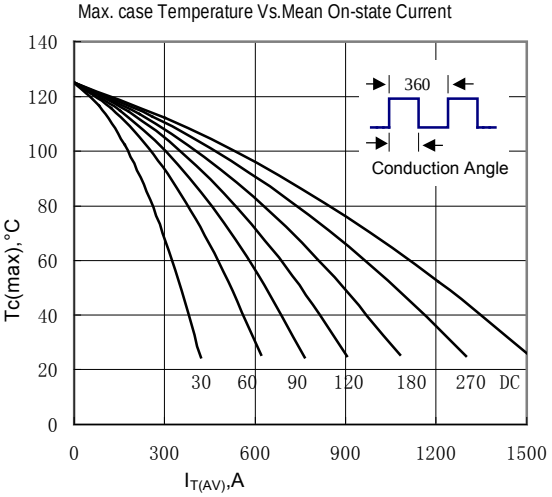


Fig.6

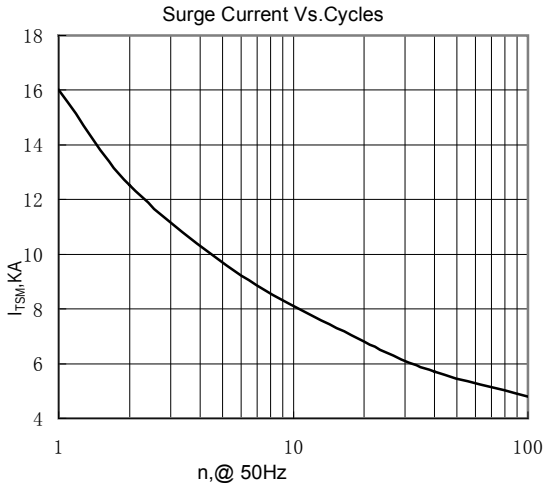


Fig.7

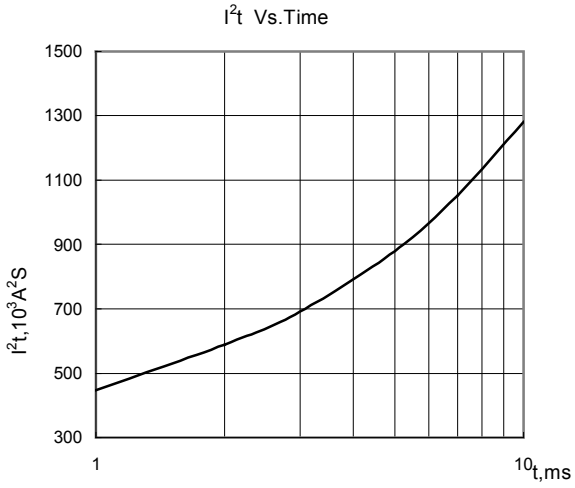


Fig.8

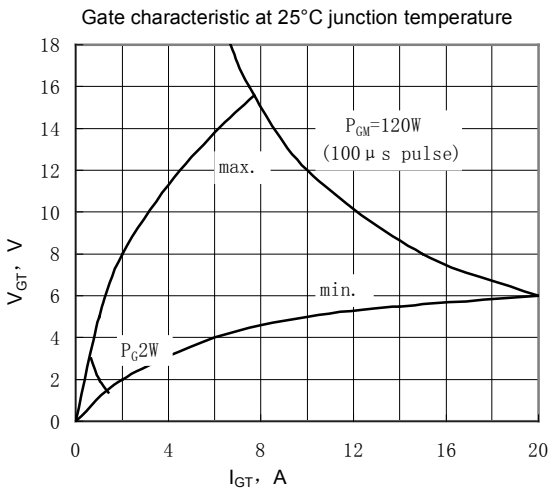


Fig.9

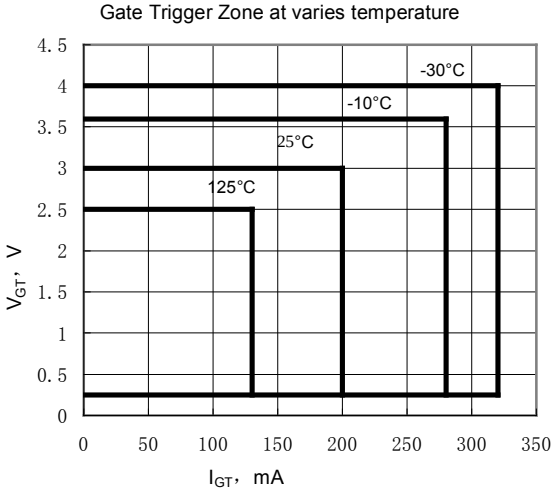


Fig.10

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